Chapter Two Differential amplifier

There are two input terminals and one output terminal. Ideally, the output signal is proportional to only the difference between the two input signals. The ideal output voltage can be written as vo = Avol(v1 −v2)

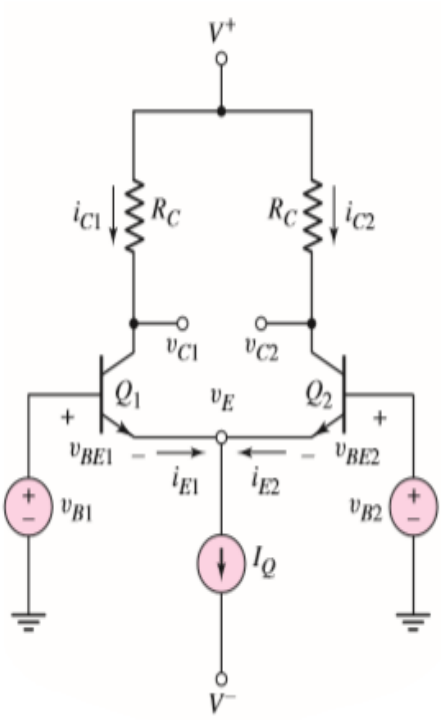
where Avol is called the open-loop voltage gain. In the ideal case, if v1 = v2, the output voltage is zero. We only obtain a nonzero output voltage if v1 and v2 are not equal. We define the differential-mode input voltage as vd = v1 −v2 and the common-mode input voltage as

$$v_{cm} = \frac{v_1 + v_2}{2}$$

These equations show that if v1 = v2, the differential-mode input signal is zero and the common-mode input signal is vcm = v1 = v2.

BJT Diff-Amp Operation

... Two identical transistors, Q_1 and Q_2, whose emitters are connected together, are biased by a constant-current source I_Q, which is connected to a negative supply voltage V^-. The collectors of Q_1 and Q_2 are connected through resistors R_C to a positive supply voltage V^+. By design, transistors Q_1 and Q_2 are to remain biased in the forward-active region. We assume that the two collector resistors R_C are equal, and that v_{B1} and v_{B2} are ideal sources, meaning that the output resistances of these sources are negligibly small.



Since both positive and negative bias voltages are used in the circuit, the need for coupling capacitors and voltage divider biasing resistors at the inputs of Q1 and Q2 has been eliminated

If the input signal voltages vB1 and vB2 in the circuit shown in Figure are both zero, Q1 and Q2 are still biased in the active region by the current source IQ. The common-emitter voltage vE would be on the order of −0.7V . This circuit, then, is referred to as a dc-coupled differential amplifier, so differences in dc input voltages can be amplified. Although the diff-amp contains two transistors, it is considered a single-stage amplifier. The analysis will show that it has characteristics similar to those of the common-emitter amplifier. First, we consider the circuit in which the two base terminals are connected together and a common-mode voltage vcm is applied as shown in Figure (a). The transistors are biased “on” by the constant-current source, and the

voltage at the common emitters is vE = vcm −VBE(on). Since Q1 and Q2 are matched or identical, current IQ splits evenly between the two transistors, and

$$i_{E1} = i_{E2} = \frac{I_Q}{2}$$

If base currents are negligible, then $i_{C1} \cong i_{E1}$ and $i_{C2} \cong i_{E2}$, and

$$v_{C1} = V^+ - \frac{I_Q}{2} R_C = v_{C2}$$

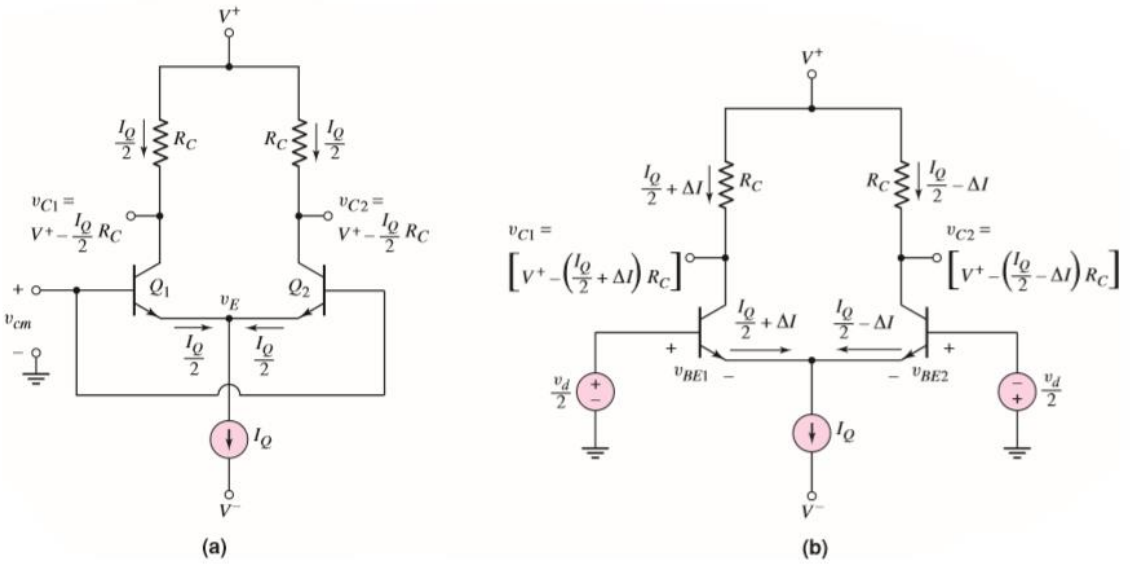


Figure (a) Basic diff-amp with applied common-mode voltage and (b) basic diff-amp with applied differential-mode voltage

for an applied common-mode voltage, IQ splits evenly between Q1 and Q2 and the difference between vC1 and vC2 is zero. Now, if vB1 increases by a few millivolts and vB2 decreases by the same amount, or vB1 = vd/2 and vB2 =− vd/2, the voltages at the bases of Q1 and Q2 are no longer equal. Since the emitters are common, this means that the B–E voltages on Q1 and Q2 are no longer equal. Since vB1 increases and vB2 decreases, then vBE1 >vBE2, which means that iC1 increases by I above its quiescent value and iC2 decreases by I below its quiescent value. A potential difference now exists between the two collector terminals. We can write

$$v_{C2} - v_{C1} = \left[V^+ - \left(\frac{I_{CQ}}{2} - \Delta I\right) R_C\right] - \left[V^+ - \left(\frac{I_{CQ}}{2} + \Delta I\right) R_C\right] = 2\Delta I R_C$$

Avoltage difference is created between vC2 and vC1 when a differential-mode input voltage is applied.

EXAMPLE 1 Determine the quiescent collector current and collector-emitter voltage in a difference amplifier. Consider the diff-amp in Figure 11.2, with circuit parameters: V+ =10 V,V − =−10 V, IQ =1 mA, and RC =10 k————————————. The transistor parameters are: β =∞ (neglect base currents), VA =∞, and VBE(on) =0.7 V. Determine iC1 and vCE1 for common-mode voltages vB1 = vB2 = vCM =0,−5V, and +5 V.

Solution: We know that iC1 =iC2 = IQ 2 =0.5mAvC1 = vC2 = V+−iC1RC =10−(0.5)(10) =5V From vCM =0,vE =− 0.7V and

vCE1 = vC1 −vE =5−(−0.7) =5.7V For vCM =−5V, vE =− 5.7Vand

vCE1 = vC1 −vE =5−(−5.7) =10.7V For vCM =+5V,vE =4.3 V and

vCE1 = vC1 −vE =5−4.3=0.7V

Small-Signal Equivalent Circuit Analysis

The dc transfer characteristics derived in the last section provide insight into the operation of the differential amplifier. Assuming we are operating in the linear range, we can also derive the gain and other characteristics of the diff-amp, using the small signal equivalent circuit.

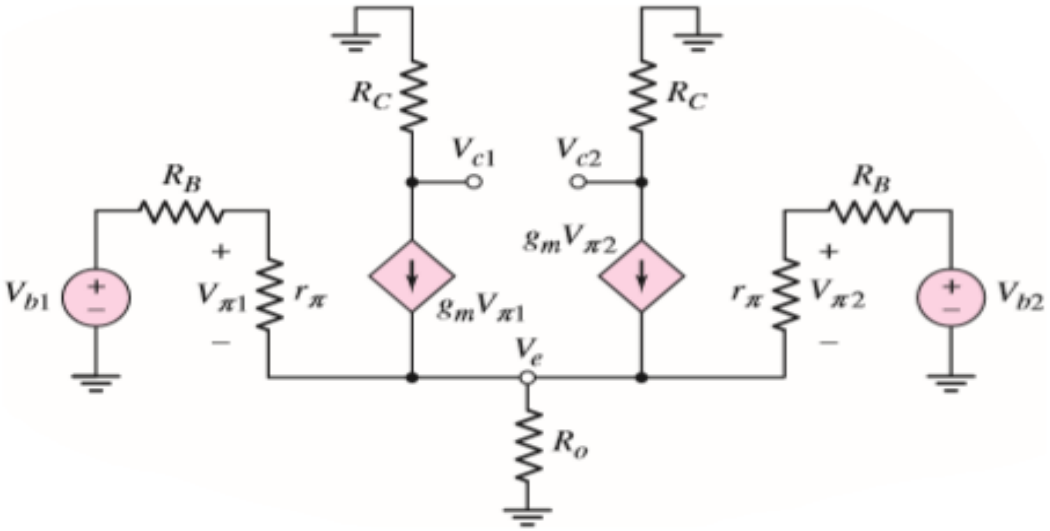


figure Small-signal equivalent circuit, bipolar differential amplifier

We assume that the Early voltage is infinite for the two emitter pair transistors, and that the constant-current source is not ideal but can be represented by a finite output impedance Ro. Resistances RB are also included. These represent the output resistance of the signal voltage sources. All voltages are represented by their phasor components. Since the two transistors are biased at the same quiescent current, we have

$$r_{\pi 1} = r_{\pi 2} \equiv r_\pi \qquad \text{and} \qquad g_{m1} = g_{m2} \equiv g_m$$

Writing a KCL equation at node V_e, using phasor notation, we have

$$\frac{V_{\pi 1}}{r_\pi} + g_m V_{\pi 1} + g_m V_{\pi 2} + \frac{V_{\pi 2}}{r_\pi} = \frac{V_e}{R_o}$$

or

$$V_{\pi 1}\left(\frac{1+\beta}{r_\pi}\right) + V_{\pi 2}\left(\frac{1+\beta}{r_\pi}\right) = \frac{V_e}{R_o}$$

where $g_m r_\pi = \beta$. From the circuit, we see that

$$\frac{V_{\pi 1}}{r_\pi} = \frac{V_{b1} - V_e}{r_\pi + R_B} \qquad \text{and} \qquad \frac{V_{\pi 2}}{r_\pi} = \frac{V_{b2} - V_e}{r_\pi + R_B}$$

Solving for $V_{\pi 1}$ and $V_{\pi 2}$ and substituting into

$$(V_{b1} + V_{b2} - 2V_e)\left(\frac{1+\beta}{r_\pi + R_B}\right) = \frac{V_e}{R_o}$$

Solving for V_e, we obtain

$$V_e = \frac{V_{b1} + V_{b2}}{2 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}}$$

One-Sided Output

If we consider a one-sided output at the collector of Q_2, then

$$V_o = V_{c2} = -(g_m V_{\pi 2})R_C = -\frac{\beta R_C (V_{b2} - V_e)}{r_\pi + R_B}$$

Substituting Equation

$$V_o = \frac{-\beta R_C}{r_\pi + R_B}\left\{\frac{V_{b2}\left[1 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}\right] - V_{b1}}{2 + \dfrac{r_\pi + R_B}{(1+\beta)R_o}}\right\}$$

In an ideal constant-current source, the output resistance is $R_o = \infty$, and Equation (11.26) reduces to

$$V_o = -\frac{\beta R_C (V_{b2} - V_{b1})}{2(r_\pi + R_B)}$$

The differential-mode input is

$$V_d = V_{b1} - V_{b2}$$

and the differential-mode gain is

$$A_d = \frac{V_o}{V_d} = \frac{\beta R_C}{2(r_\pi + R_B)}$$

, we can solve these equations for V_{b1} and V_{b2} in terms of V_d and V_{cm}. We obtain

$$V_{b1} = V_{cm} + \frac{V_d}{2}$$

and

$$V_{b2} = V_{cm} - \frac{V_d}{2}$$

$$V_o = \frac{\beta R_C}{2(r_\pi + R_B)} \cdot V_d - \frac{\beta R_C}{r_\pi + R_B + 2(1+\beta)R_o} \cdot V_{cm}$$

We can write the output voltage in the general form

$$V_o = A_d V_d + A_{cm} V_{cm}$$

where Ad is the differential-mode gain and Acm is the common-mode gain

$$A_d = \frac{\beta R_C}{2(r_\pi + R_B)}$$

and the common-mode gain is

$$A_{cm} = \frac{-\beta R_C}{r_\pi + R_B + 2(1+\beta)R_o}$$

We again observe that the common-mode gain goes to zero for an ideal current source in which $R_o = \infty$. For a nonideal current source, R_o is finite and the common-mode gain is not zero for this case of a one-sided output. A nonzero common-mode gain implies that the diff-amp is not ideal.

Common-Mode Rejection Ratio

The ability of a differential amplifier to reject a common-mode signal is described in terms of the common-mode rejection ratio (CMRR). The CMRR is a figure of merit for the diff-amp and is defined as

$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right|$$

For an ideal diff-amp, $A_{cm} = 0$ and $\text{CMRR} = \infty$. Usually, the CMRR is expressed in decibels, as follows:

$$\text{CMMR}_{\text{dB}} = 20 \log_{10}\left|\frac{A_d}{A_{cm}}\right|$$

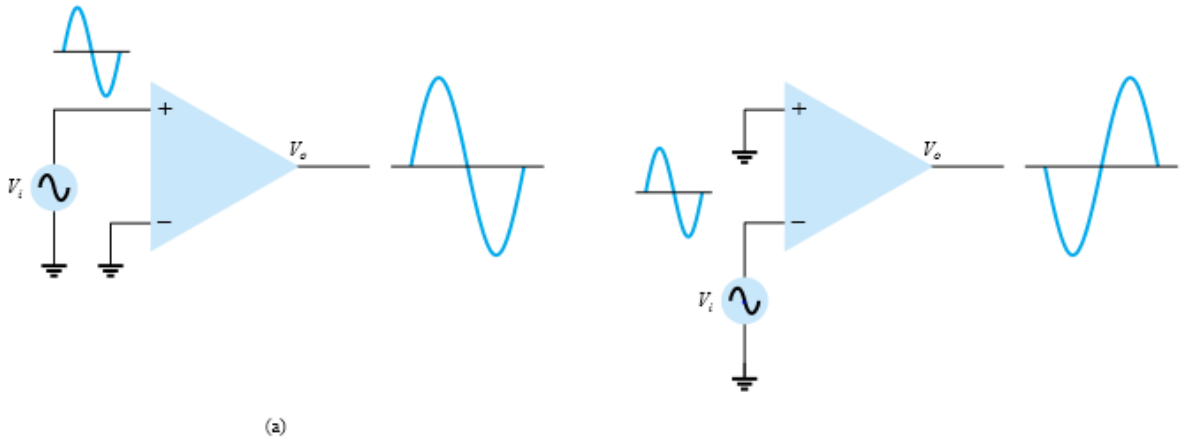
$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| = \frac{1}{2}\left[1 + \frac{2(1+\beta)R_o}{r_\pi + R_B}\right]$$

The common-mode gain decreases as R_o increases. Therefore, we see that the CMRR increases as R_o increases.

Input and Output of a differential amplifier

Single-Ended Input

Single-ended input operation results when the input signal is connected to one input with the other input connected to ground.

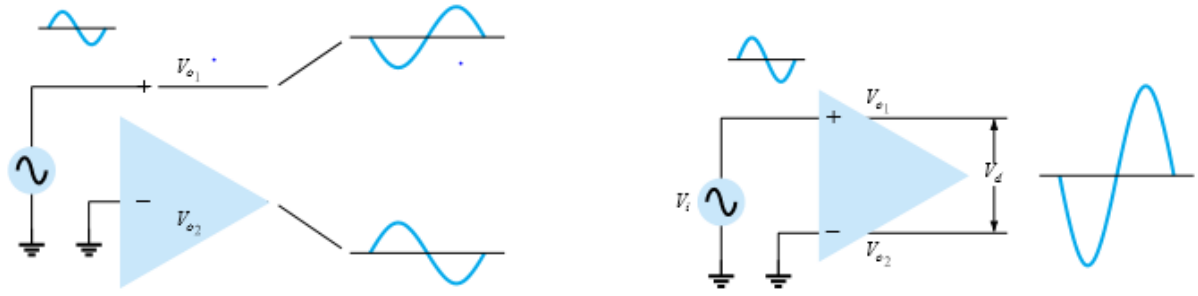


(a)

For this operation. In Fig. a, the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Figure b shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.

Double-Ended Output

While the operation discussed so far had a single output, the op-amp can also be operated with opposite outputs, as shown in Fig. An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Figure shows a single-ended input with a double-ended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. The same operation with a single output measured between output terminals (not with respect to ground). This difference output signal is Vo1 -Vo2. The difference output is also referred to as a floating signal since neither output terminal is the ground (reference) terminal. Notice that the difference output is twice as large as either Vo1 or Vo2 since they are of opposite polarity and subtracting them results in twice their amplitude Figure shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.



Differential- and Common-Mode Gains

For greater insight into the mechanism that causes differential- and common-mode gains, we reconsider the diff-amp as pure differential- and common-mode signals are applied. Figure shows the ac equivalent circuit of the diff-amp with two sinusoidal input signals. The two input voltages are 180 degrees out of phase, so a pure differential-mode signal is being applied to the diff-amp. We see that vb1 +vb2 =0. From Equation we find ve =0,so the common emitters of Q1 and Q2 remain at signal ground. In essence, the circuit behaves like a balanced seesaw. As the base voltage of Q1 goes into its positive-half cycle, the base voltage of Q2 is in its negative half-cycle. Then, as the base voltage of Q1 goes into its negative half-cycle, the base voltage of Q2 is in its positive half-cycle. The signal current directions shown in the figure are valid for vb1 in its positive half-cycle.

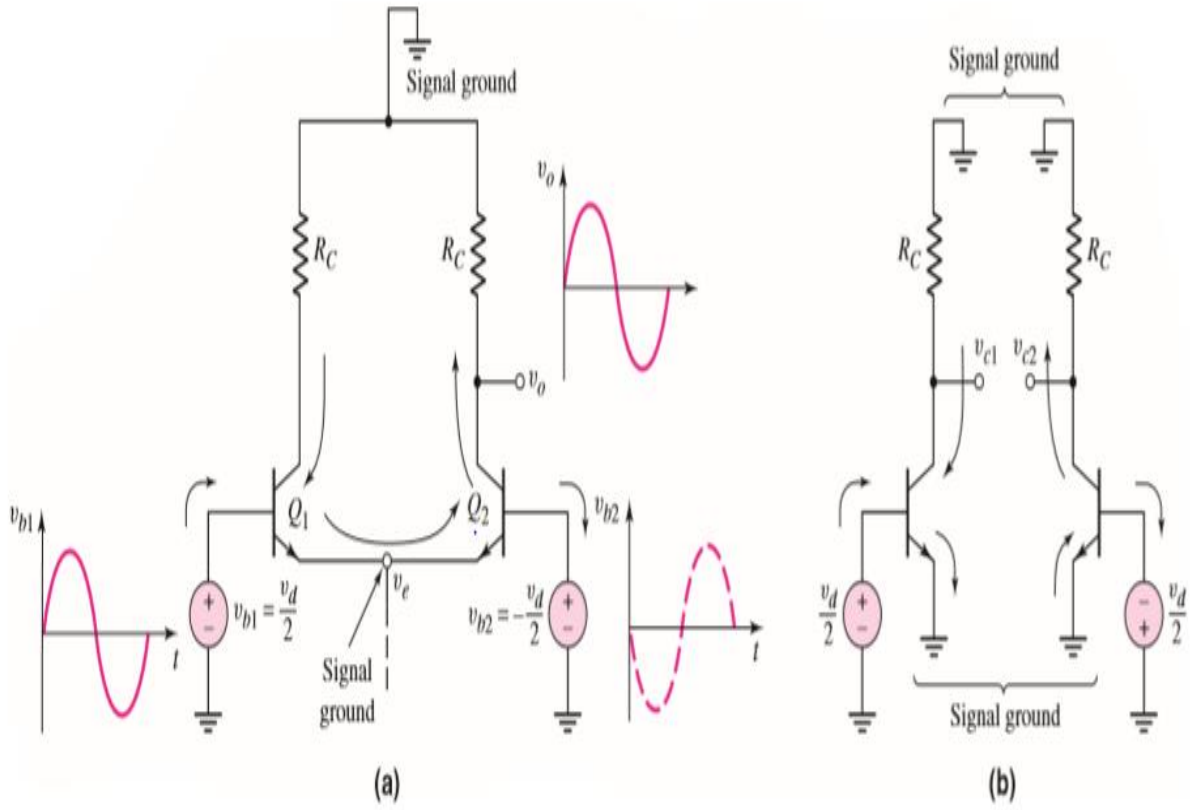


Figure (a) Equivalent ac circuit, diff-amp with applied sinusoidal differential-mode input signal, and resulting signal current directions and (b) differential-mode half-circuits

Since ve is always at ground potential, we can treat each half of the diff-amp as a common-emitter circuit. Figure (b) shows the differential half-circuits, clearly depicting the common-emitter configuration. The differential-mode characteristics of the diff-amp can be determined by analyzing the half-circuit. In evaluating the small-signal hybrid-π parameters, we must keep in

mind that the half-circuit is biased at IQ/2. Figure below (a) shows the ac equivalent circuit of the diff-amp with a pure common-mode sinusoidal input signal. In this case, the two input voltages are in phase. The current source is represented as an ideal source IQ in parallel with its output resistance Ro. Current iq is the time-varying component of the source current. As the two input signals increase, voltage ve increases and current iq increases. Since this current splits evenly between Q1 and Q2, each collector current also increases. The output voltage vo then decreases below its quiescent value. As the two input voltages go through the negative half-cycle, all signal currents shown in the figure reverse direction, and vo increases above its quiescent value.

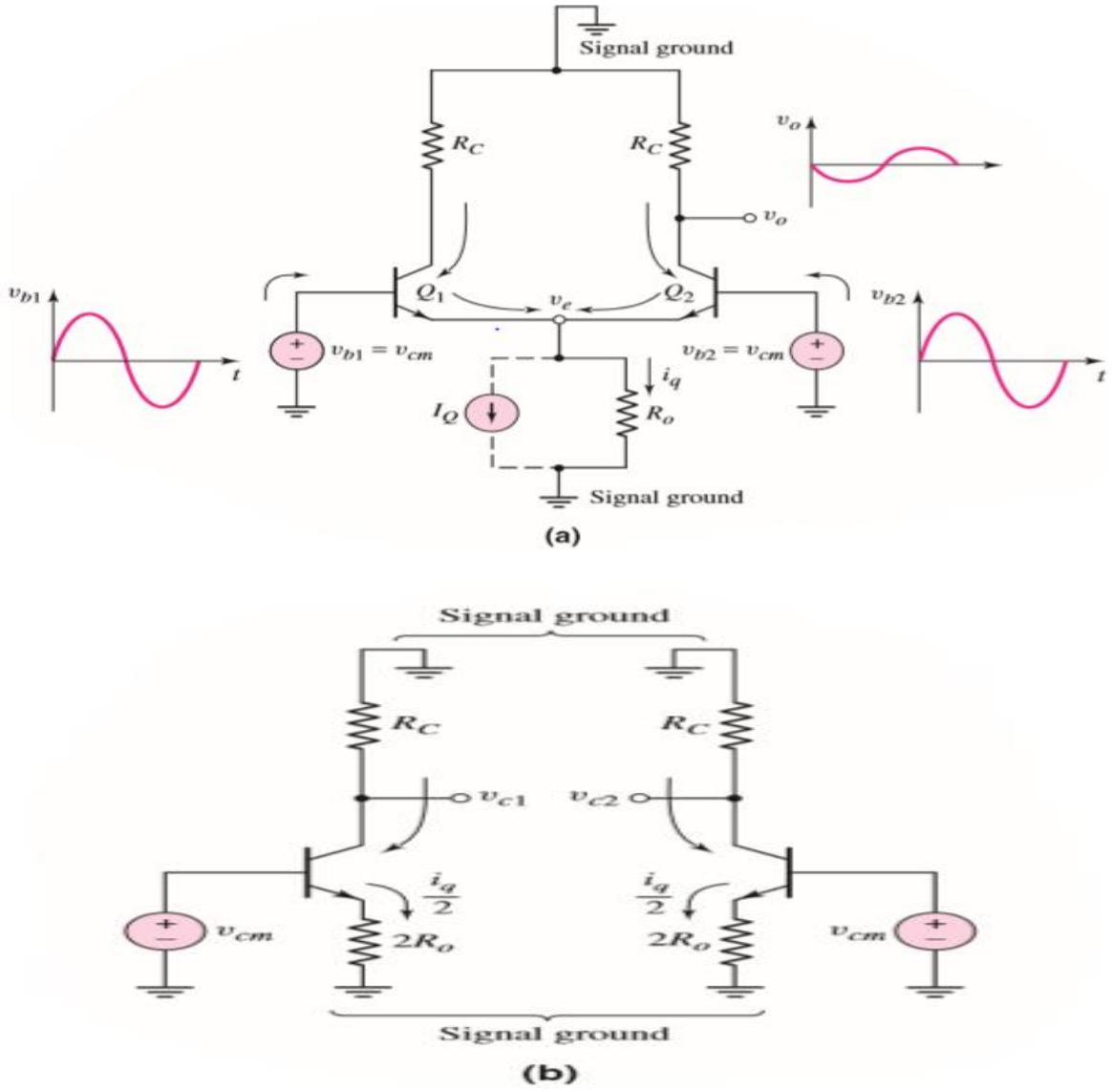


Figure (a) Equivalent ac circuit of diff-amp with common-mode input signal, and resulting signal current directions and (b) common-mode half-circuits

Consequently, a common-mode sinusoidal input signal produces a sinusoidal output voltage, which means that the diff-amp has a nonzero common-mode voltage gain. If the value of Ro increases, the magnitude of iq decreases for a given common-mode input signal, producing a smaller output voltage and hence a smaller common-mode gain. With an applied common-mode voltage, the circuit shown in Figure (a) above is perfectly symmetrical. The circuit can therefore be split into the identical common mode half-circuits shown in Figure (b) above. The common-mode characteristics of the diff-amp can then be determined by analyzing the half-circuit, which is a common emitter configuration with an emitter resistor. Each half-circuit is biased atIQ/2.

Differential- and Common-Mode Input Impedances

The input impedance, or resistance, of an amplifier is as important a property as the voltage gain. The input resistance determines the loading effect of the circuit on the signal source. We will look at two input resistances for the difference amplifier: the differential-mode input resistance, which is the resistance seen by a differential mode signal source; and the common-mode input resistance, which is the resistance seen by a common-mode input signal source.

Differential-Mode Input Resistance

The differential-mode input resistance is the effective resistance between the two input base terminals when a differential-mode signal is applied.

$$\frac{v_d/2}{i_b} = r_\pi$$

The differential-mode input resistance is therefore

$$R_{id} = \frac{v_d}{i_b} = 2r_\pi$$

Another common diff-amp configuration uses emitter resistors, as shown in Figure 11.15. With a pure applied differential-mode voltage, similar differential-mode half-circuits are applicable to this configuration. We can then use the resistance reflection rule to find the differential-mode input resistance. We have

$$\frac{v_d/2}{i_b} = r_\pi + (1+\beta)R_E$$

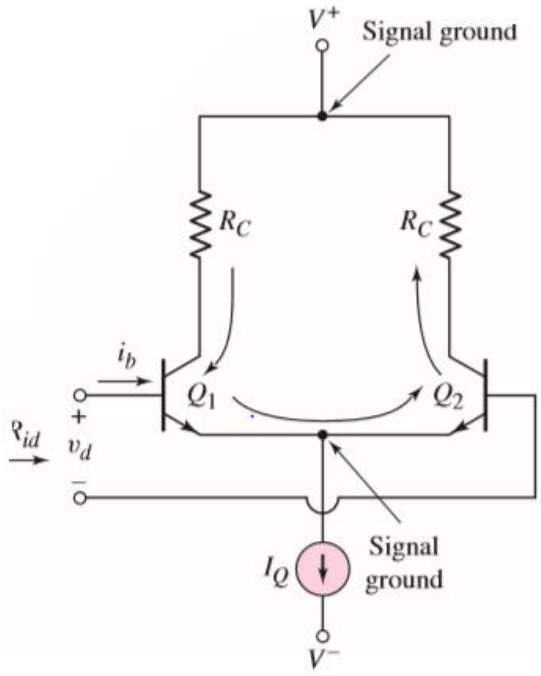


Figure 11.14 BJT differential amplifier with differential-mode input signal, showing differential input resistance

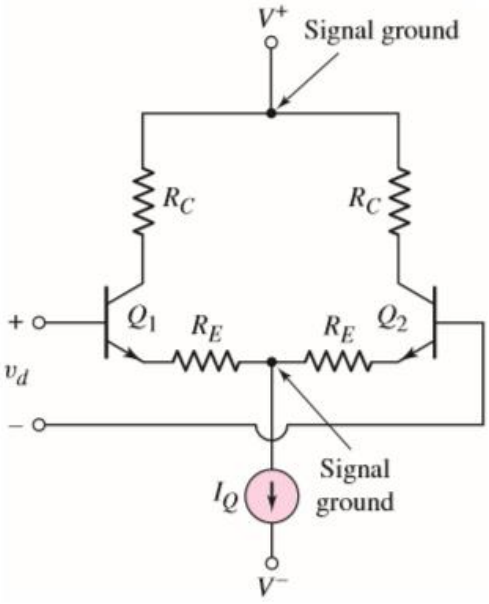


Figure 11.15 BJT differential amplifier with emitter resistors

Therefore,

$$R_{id} = \frac{v_d}{i_b} = 2[r_\pi + (1+\beta)R_E]$$

Equation (11.53) implies that the differential-mode input resistance increases significantly when emitter resistors are included. We will see that the differential-mode gain decreases when emitter resistors are included in the same way that the voltage gain of a common-emitter amplifier decreases when an emitter resistor is included in the design. However, a larger differential-mode voltage (greater than 18 mV) may be applied to the diff-amp in Figure 11.15 and the amplifier remains linear.

Common-Mode Input Resistance

Figure 11.16(a) shows a diff-amp with an applied common-mode voltage. The small-signal output resistance R_o of the constant-current source is also shown. The equivalent common-mode half-circuits were given in Figure 11.13(b). Since the half-circuits are in parallel, we can write

$$2R_{icm} = r_\pi + (1+\beta)(2R_o) \cong (1+\beta)(2R_o)$$

a first approximation for determining the common-mode input

Normally, R_o is large, and R_{icm} is typically in the megohm range. Therefore, the transistor output resistance r_o and the base–collector resistance r_μ may need to be included in the calculation. Figure 11.16(b) shows the more complete equivalent half-circuit model. For this model, we have

$$2R_{icm} = r_\mu \,\|[(1+\beta)(2R_o)]\|\,[(1+\beta)r_o]$$

Therefore,

$$R_{icm} = \left(\frac{r_\mu}{2}\right)\|[(1+\beta)(R_o)]\|\left[(1+\beta)\left(\frac{r_o}{2}\right)\right]$$

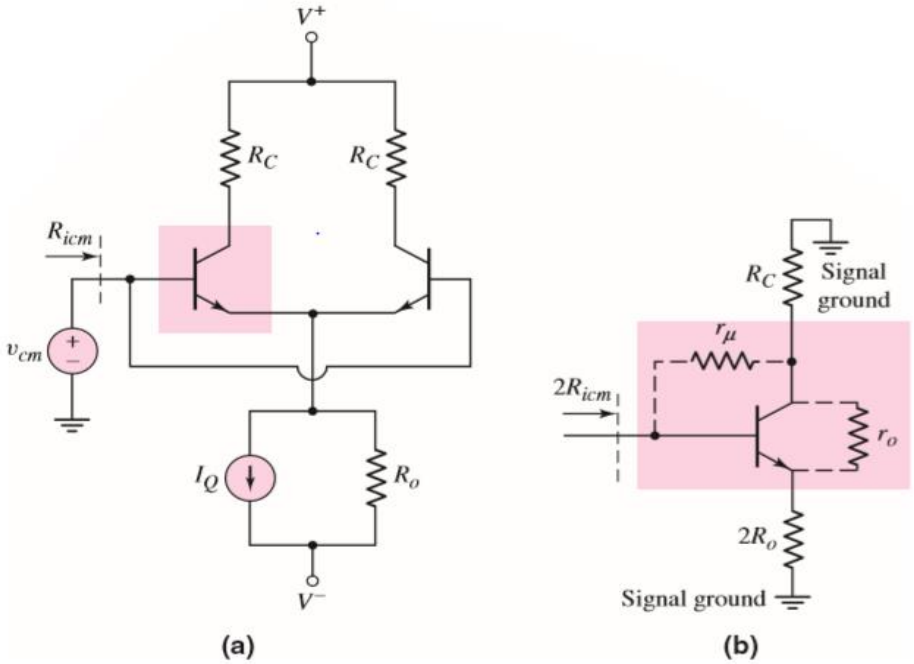


Figure 11.16 (a) BJT differential amplifier with common-mode input signal, including finite current source resistance and (b) equivalent common-mode half-circuit

EXAMPLE 11.6

Objective: Determine the differential- and common-mode input resistances of a differential amplifier.

Consider the circuit in Figure 11.17, with transistor parameters $\beta = 100$, $V_{BE}(\text{on}) = 0.7$ V, and $V_A = 100$ V. Determine R_{id} and R_{icm}.

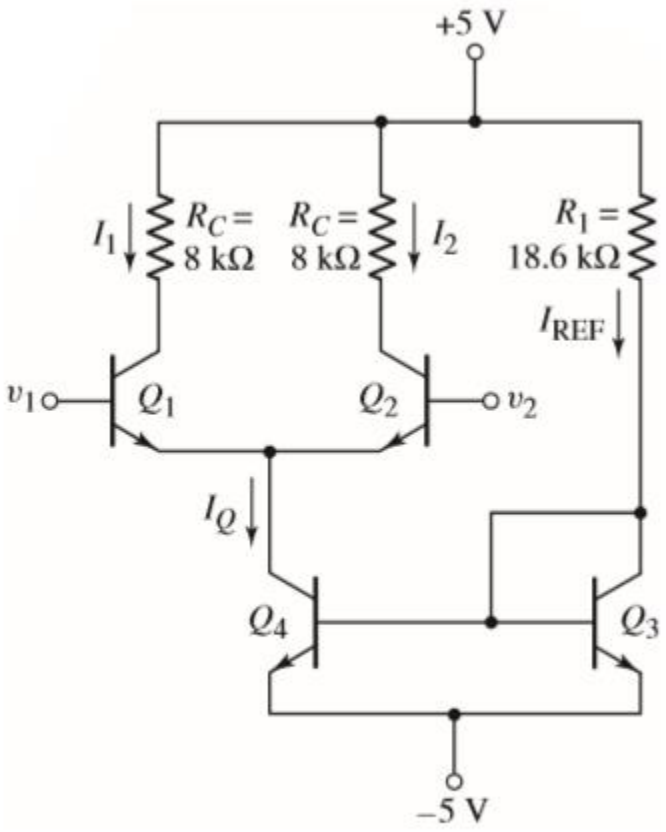


Figure 11.17 BJT differential amplifier for Example 11.6

Solution: From the circuit, we find

$$I_{\text{REF}} = 0.5\,\text{mA} \cong I_Q$$

and

$$I_1 = I_2 \cong I_Q/2 = 0.25\,\text{mA}$$

The small-signal parameters for Q_1 and Q_2 are then

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(100)(0.026)}{0.25} = 10.4\,\text{k}\Omega$$

and

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{0.25} = 400\,\text{k}\Omega$$

and the output resistance of Q_4 is

$$R_o = \frac{V_A}{I_Q} = \frac{100}{0.5} = 200\,\text{k}\Omega$$

From Equation (11.51), the differential-mode input resistance is

$$R_{id} = 2r_\pi = 2(10.4) = 20.8\,\text{k}\Omega$$

From Equation (11.55(b)), neglecting the effect of r_μ, the common-mode input resistance is

$$R_{icm} = (1+\beta)\left[(R_o)\left\|\left(\frac{r_o}{2}\right)\right.\right] = (101)\left\{200\left\|\left(\frac{400}{2}\right)\right.\right\}\text{k}\Omega \rightarrow 10.1\,\text{M}\Omega$$

EXERCISE PROBLEM

Ex 11.6: Consider the diff-amp shown in Figure 11.15. Assume the current source has a value of $I_Q = 0.5$ mA, the transistor current gains are $\beta = 100$, and the emitter resistors are $R_E = 500\,\Omega$. Find the differential input resistance. (Ans. $R_{id} = 122\,\text{k}\Omega$)

Differential-Mode Voltage Gain with Emitter Degeneration

We may determine the differential-mode voltage gain of the circuit shown in Figure 11.15. Figure 11.18 shows the differential-mode half circuits. For a one-sided output and for matched elements, we have

$$V_o = V_{c2} = -g_m V_{\pi 2} R_C$$

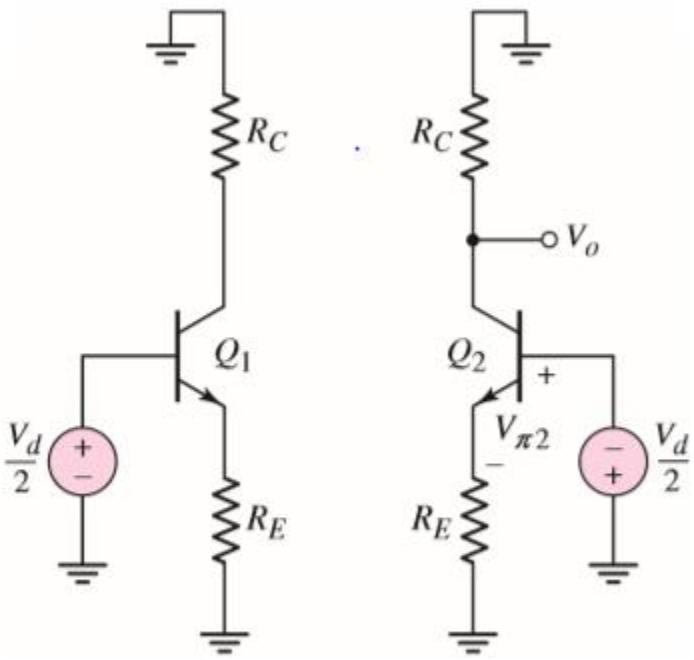


Figure 11.18 Differential half-circuits with emitter degeneration

Writing a KVL equation around the B–E loop, we have

$$\frac{V_d}{2} + V_{\pi 2} + g_m V_{\pi 2} R_E = 0$$

which yields

$$V_{\pi 2} = \frac{-(V_d/2)}{1 + g_m R_E}$$

Substituting Equation (11.58) into (11.56), we find the differential-mode voltage gain as

$$A_d = \frac{V_o}{V_d} = \frac{g_m R_C}{2(1 + g_m R_E)}$$

EXAMPLE 11.7

Objective: Determine the one-sided differential-mode voltage gain of the circuit shown in Figure 11.15.

Assume $I_Q = 0.5\,\text{mA}$, $\beta = 100$, and $R_C = 10\,\text{k}\Omega$. Find the differential-mode voltage gain for (a) $R_E = 0$ and (b) $R_E = 500\,\Omega$.

Solution: The small-signal transconductance is found to be $g_m = 9.62\,\text{mA/V}$. We find the differential-mode voltage gain to be (a) for $R_E = 0$:

$$A_d = \frac{g_m R_C}{2} = \frac{(9.62)(10)}{2} = 48.1$$

and (b) for $R_E = 500\,\Omega$:

$$A_d = \frac{g_m R_C}{2(1 + g_m R_E)} = \frac{(9.62)(10)}{2[1 + (9.62)(0.5)]} = 8.28$$

EXERCISE PROBLEM

Ex 11.7: Consider the diff-amp described in Example 11.7. Assume the same parameters except the value of R_E. Determine the value of R_E that results in a differential-mode voltage gain of $A_d = 10$. What is the corresponding value of differential-input resistance? (Ans. $R_E = 0.396\,\text{k}\Omega$, $R_{id} = 100.8\,\text{k}\Omega$)

BASIC FET DIFFERENTIAL PAIR

Objective: • Describe the characteristics of and analyze the basic FET differential amplifier.

In this section, we will evaluate the basic FET differential amplifier, concentrating on the MOSFET diff-amp. As we did for the bipolar diff-amp, we will develop the dc transfer characteristics, and determine the differential- and common-mode gains.

Differential amplifiers using JFETs are also available. Since the analysis is almost identical to that for the MOSFET diff-amp, we will only briefly consider the JFET differential pair. A few of the problems at the end of this chapter are based on these circuits.

DC Transfer Characteristics

Figure 11.19 shows the basic MOSFET differential pair, with matched transistors M_1 and M_2 biased with a constant current I_Q. We assume that M_1 and M_2 are always biased in the saturation region.

Like the basic bipolar configuration, the basic MOSFET diff-amp uses both positive and negative bias voltages, thereby eliminating the need for coupling capacitors and voltage divider biasing resistors at the gate terminals. Even with $v_{G1} = v_{G2} = 0$, the transistors M_1 and M_2 can be biased in the saturation region by the current source I_Q. This circuit, then, is also a **dc-coupled** diff-amp.

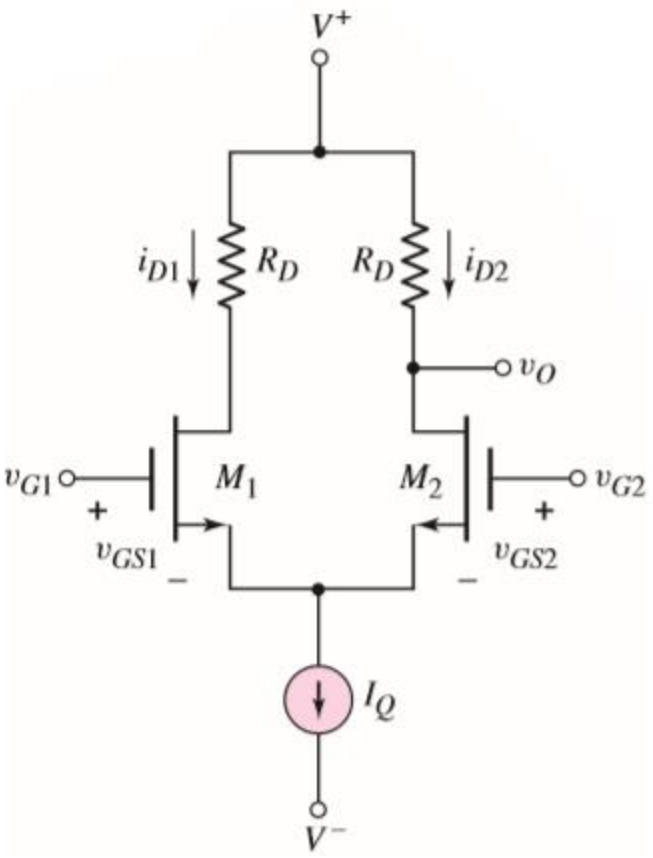


Figure 11.19 Basic MOSFET differential pair configuration

EXAMPLE 11.8

Objective: Calculate the dc characteristics of a MOSFET diff-amp.

Consider the differential amplifier shown in Figure 11.20. The transistor parameters are: $K_{n1} = K_{n2} = 0.1$ mA/V^2, $K_{n3} = K_{n4} = 0.3$ mA/V^2, and for all transistors, $\lambda = 0$ and $V_{TN} = 1$ V. Determine the maximum range of common-mode input voltage.

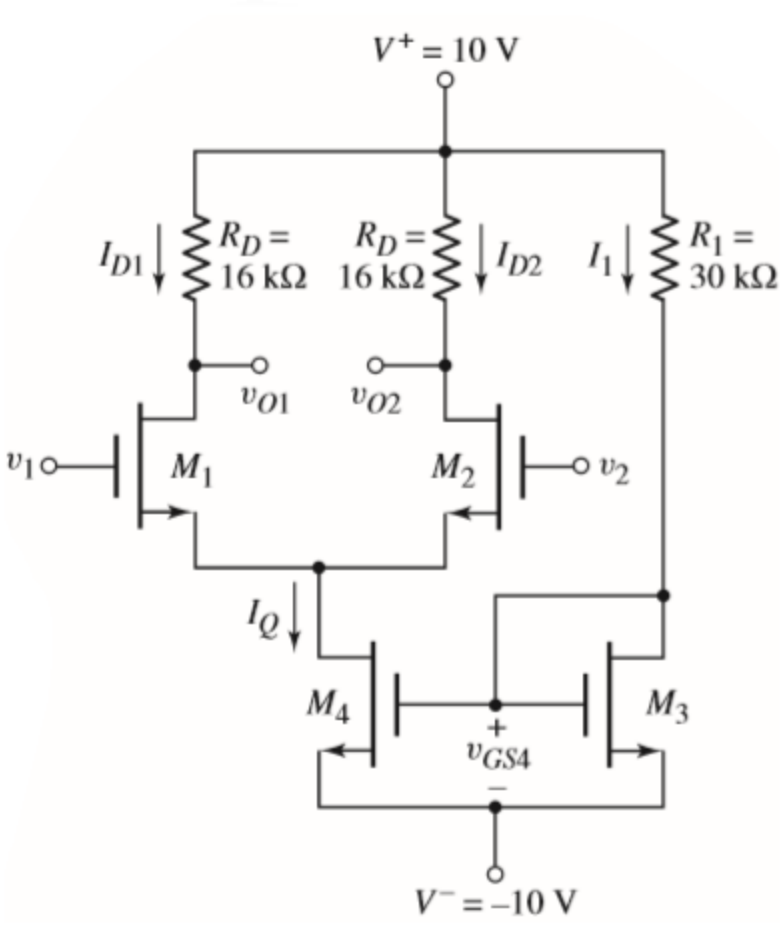


Figure 11.20 MOSFET differential amplifier for Example 11.8

Solution: The reference current can be determined from

$$I_1 = \frac{20 - V_{GS4}}{R_1}$$

and from

$$I_1 = K_{n3}(V_{GS4} - V_{TN})^2$$

Combining these two equations and substituting the parameter values, we obtain

$$9V_{GS4}^2 - 17V_{GS4} - 11 = 0$$

which yields

$$V_{GS4} = 2.40\ \text{V} \qquad \text{and} \qquad I_1 = 0.587\ \text{mA}$$

Since M_3 and M_4 are identical, we also find

$$I_Q = 0.587\ \text{mA}$$

The quiescent drain currents in M_1 and M_2 are

$$I_{D1} = I_{D2} = I_Q/2 \cong 0.293\ \text{mA}$$

The gate-to-source voltages are ther

$$V_{GS1} = V_{GS2} = \sqrt{\frac{I_{D1}}{K_{n1}}} + V_{TN} = \sqrt{\frac{0.293}{0.1}} + 1 = 2.71\ \text{V}$$

The quiescent values of v_{O1} and v_{O2} are

$$v_{O1} = v_{O2} = 10 - I_{D1}R_D = 10 - (0.293)(16) = 5.31\,\text{V}$$

The maximum common-mode input voltage is the value when M_1 and M_2 reach the transition point, or

$$V_{DS1} = V_{DS2} = V_{DS1}(\text{sat}) = V_{GS1} - V_{TN} = 2.71 - 1 = 1.71\,\text{V}$$

Therefore,

$$v_{CM}(\text{max}) = v_{O1} - V_{DS1}(\text{sat}) + V_{GS1} = 5.31 - 1.71 + 2.71$$

or

$$v_{CM}(\text{max}) = 6.31\,\text{V}$$

The minimum common-mode input voltage is the value when M_4 reaches the transition point, or

$$V_{DS4} = V_{DS4}(\text{sat}) = V_{GS4} - V_{TN} = 2.4 - 1 = 1.4\,\text{V}$$

Therefore,

$$v_{CM}(\text{min}) = V_{GS1} + V_{DS4}(\text{sat}) - 10 = 2.71 + 1.4 - 10$$

or

$$v_{CM}(\text{min}) = -5.89\,\text{V}$$

EXERCISE PROBLEM

***Ex 11.8:** For the differential amplifier in Figure 11.20, the parameters are: $V^+ = 5\,\text{V}$, $V^- = -5\,\text{V}$, $R_1 = 80\,\text{k}\Omega$, and $R_D = 40\,\text{k}\Omega$. The transistor parameters are $\lambda = 0$ and $V_{TN} = 0.8\,\text{V}$ for all transistors, and $K_{n3} = K_{n4} = 100\,\mu\text{A/V}^2$ and $K_{n1} = K_{n2} = 50\,\mu\text{A/V}^2$. Determine the range of the common-mode input voltage. (Ans. $-2.18 \le v_{cm} \le 3.76\,\text{V}$)